<u>S/N 10/789,882</u> <u>PATENT</u>

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Paul A. Farrar

Examiner: Dao H. Nguyen

Serial No.:

10/789,882

Group Art Unit: 2818

Filed:

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Docket: 303.673US3

Title:

INTEGRATED CIRCUIT AND SEED LAYERS

COMMUNICATION CONCERNING RELATED APPLICATION(S)

MS Amendment

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Applicant would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

<u>Serial/Patent No.</u> 09/488098 6429120	Filing Date/Issue Date January 18, 2000	Attorney Docket 303.618US1	Title METHOD AND APPARATUS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALS
09/484303 7262130	January 18, 2000	303.648US1	METHODS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALS
09/483869 6420262	January 18, 2000	303.664US1	STRUCTURES AND METHODS TO ENHANCE COPPER METALLIZATION
09/483881 7211512	January 18, 2000	303.672US1	SELECTIVE ELECTROLESS-PLATED COPPER METALLIZATION
09/484002 6376370	January 18, 2000	303.673US1	PROCESS FOR PROVIDING SEED LAYERS FOR USING ALUMINUM, COPPER, GOLD AND SILVER METALLURGY
10/117041 7105914	April 5, 2002	303.673US2	INTEGRATED CIRCUIT AND SEED LAYERS
10/196078 6743716	July 16, 2002	303.664US2	STRUCTURES AND METHODS TO ENHANCE COPPER METALLIZATION
10/196081 20020182859A1	July 16, 2002	303.664US3	STRUCTURES AND METHODS TO ENHANCE COPPER METALLIZATION
10/211855 6756298	August 1, 2002	303.618US2	METHODS AND APPARATUS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALS

Page 2 Dkt: 303.673US3

THE, INTEGRATED CIRCUIT AND SEED LATERS					
10/842042 7285196	May 7, 2004	303.618US3	METHODS AND APPARATUS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALS		
10/195965 20020177302A1	July 16, 2002	303.664US4	STRUCTURES AND METHODS TO ENHANCE COPPER METALLIZATION		
10/634274 7220665	August 5, 2003	1303.110US1	H2 PLASMA TREATMENT		
10/854552	May 26, 2004	303.664US5	STRUCTURES AND METHODS TO ENHANCE COPPER METALLIZATION		
10/929251 7262505	August 30, 2004	303.672US2	SELECTIVE ELECTROLESS-PLATED COPPER METALLIZATION		
10/931541 7253521	August 31, 2004	303.648US2	METHODS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALS		
11/215367 20060006548A1	August 29, 2005	1303.110US2	ELECTRONIC APPARATUS HAVING A CORE CONDUCTIVE STRUCTURE WITHIN AN INSULATING LAYER (as amended)		
11/457099 20060246733A1	July 12, 2006	303.648US3	METHOD FOR MAKING INTEGRATED CIRCUITS		
11/458975 20060292857A1	July 20, 2006	303.648US4	METHODS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALS		
11/458195 20060255462A1	July 18, 2006	303.664US6	STRUCTURES AND METHODS TO ENHANCE COPPER METALLIZATION		
11/639020 20070085213A1	December 14, 2006	303.672US3	SELECTIVE ELECTROLESS-PLATED COPPER METALLIZATION		
11/652310 20070141830A1	January 11, 2007	303.648US5	METHODS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALS		
11/706662 20070167005A1	February 15, 2007	303.672US4	SELECTIVE ELECTROLESS-PLATED COPPER METALLIZATION		

Continuations and divisionals may be later filed on the cases listed above, or cited to the Examiner in any previous Communication Concerning Related Applications. Applicants request that the Examiner review all continuations and divisionals of the above-listed or previously-cited patent applications before allowing the claims of the present patent application.

Respectfully submitted,

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.

P.O. Box 2938

Minneapolis, MN 55402

(612) 371-2157

Date 30 October 2007 By

David R. Cochran Reg. No. 46,632

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this Cotober, 2007.

Judy Dent

Signature